BITSTREAM →

Data ordering	→	Arithmetic coding	→	Coefficient bit modeling	→	Quantization	→	wavelet Transform	→	DC Level shifting multiple component transform
101		102		103		104		106		107

ROI
105

Reconstructed and rendered image

Figure 1

SP 0	SP 4	C 8	C 12	C 16	C 20	C 24	C 28
R 1	SP 5	C 9	C 13	C 17	C 21	C 25	C 29
R 2	SP 6	SP 10	SP 14	SP 18	C 22	C 26	C 30
SP 3	SP 7	R 11	R 15	SP 19	C 23	C 27	C 31
C 32	SP 36	SP 40	SP 44	SP 48	C 52	C 56	C 60
C 33	C 37	C 41	C 45	C 49	C 53	C 57	C 61
C 34	C 38	C 42	C 46	C 50	C 54	C 58	C 62
C 25	C 39	C 43	C 47	C 51	C 55	C 59	C 63

Figure 2A

run counts　　　　unused memoy　　　　skip counts

Figure 2B

311
312
313
314

(A)　　　　(B)　　　　(C)　　　　(D)
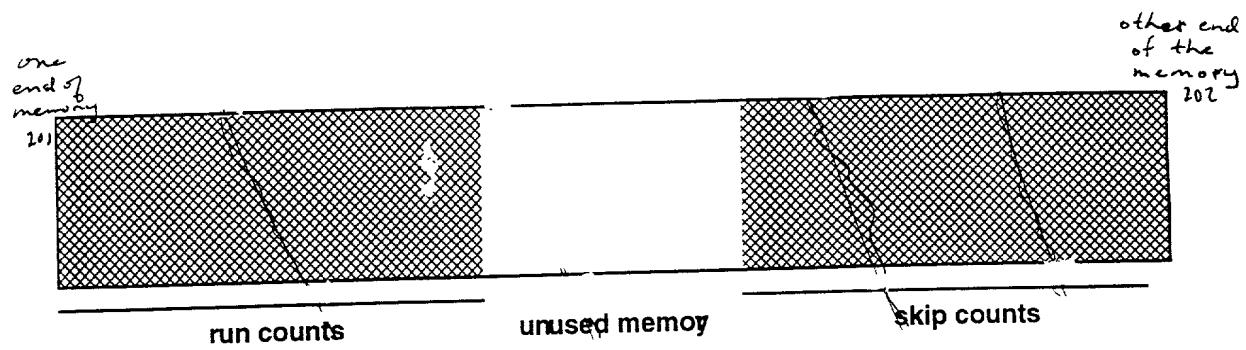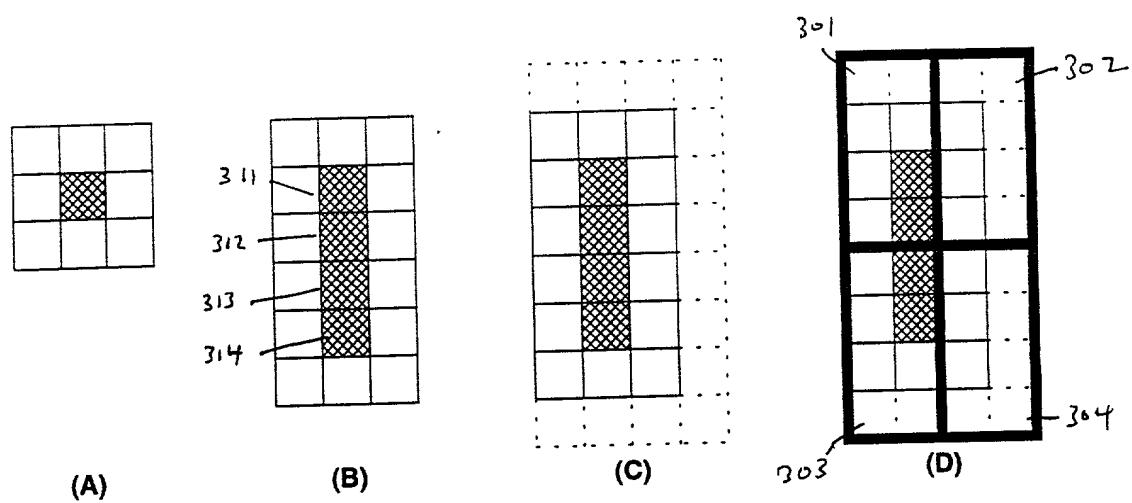
Figure 3

	0	1	2	3	4	5	6	7
0	A	B	A	B	A	B	A	B
1	C	D	C	D	C	D	C	D
2	A	B	A	B	A	B	A	B
3	C	D	C	D	C	D	C	D
0	A	B	A	B	A	B	A	B

Figure 4

address A | memory A | data out | register 501

address B | memory B | data out | register 502

address C | memory C | data out | register 503

address D | memory D | data out | register 504

Figure 5

501   502   A   B

603

601

602

503   604   504   C   D

Figure 6

pass for 4x4 region

significance
propagation
703

significance
state for 8x8
region
701

708

count

determine
pass
702

refinement

704

mask
705

16

priority
encode
706

16

cleanup

705

16

16

SELECTION
(mux)
LOGIC
707

1

16

1

control
709

refinement next index

refinement run

refinement skip

cleanup next index

cleanup run

cleanup skip

signif prop

Figure 7

SP	SP	SP	SP
C	C	C	C
SP	SP	SP	SP
SP	R	R	SP

SP = significance propagtion
C = cleanup
R = refinement

SP pass: 10*2 for SP pass coefcients
          6 for C and R pass coefcients
C pass: 4*2 for C pass coeficients
R pass: 2 for R pass

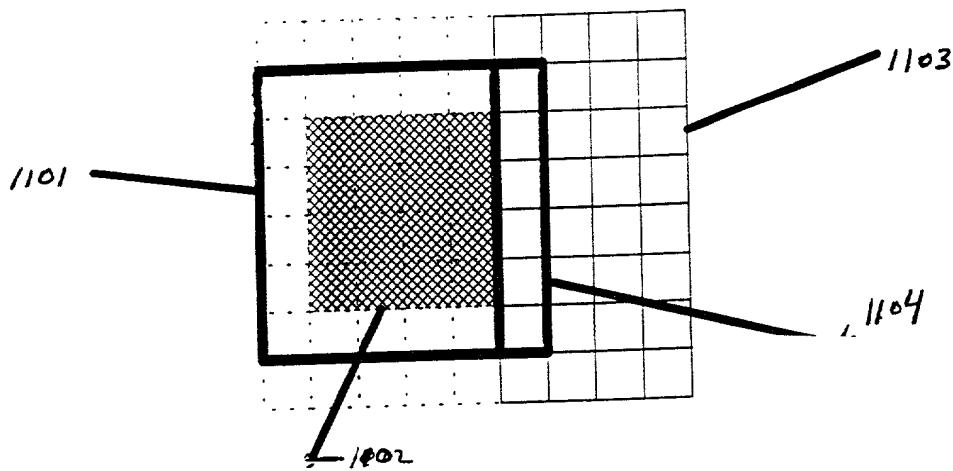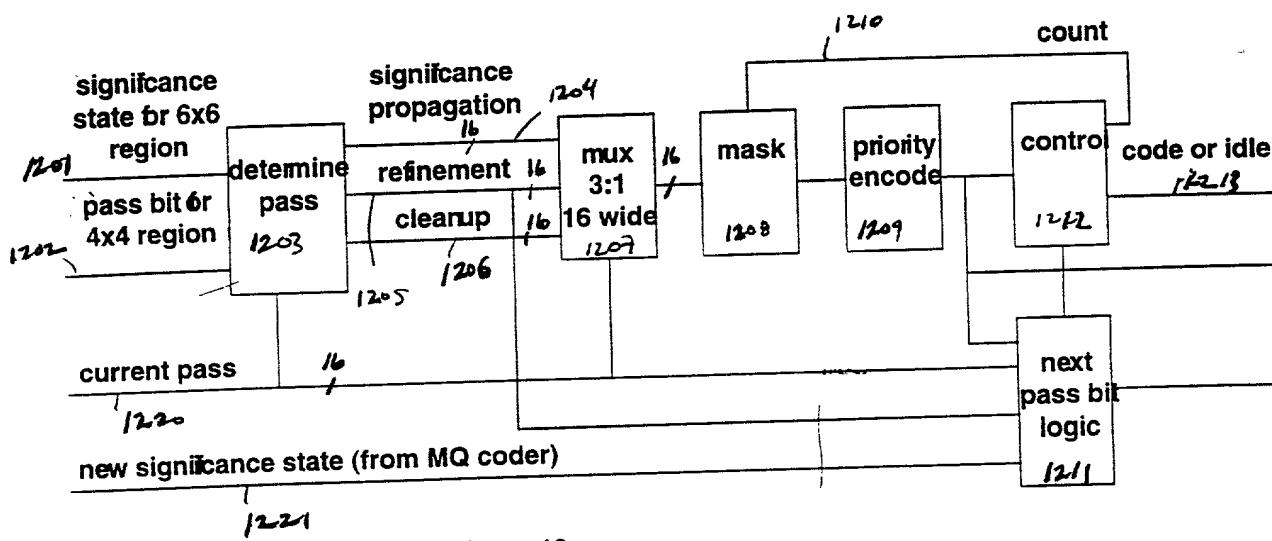total: 36 clocks = 2.25 clocks per coefcient

Figure 8

Figure 9

Figure 10

1103

1101

1104

1002

Figure 11

significance
state for 6x6
region

1201

pass bit for
4x4 region

1202

determine
pass

1203

significance
propagation

1204

refinement 16

cleanup 16

1205   1206

16

mux
3:1
16 wide

1207

16

mask

1208

1210   count

priority
encode

1209

control

1212

code or idle

1213

current pass 16

1220

next
pass bit
logic

1211

new significance state (from MQ coder)

1221

Figure 12

context 0

enable 0

context

bit

context
model

1301

context 1

mux

1302

enable

MQ-coder

1303

enable 1

Figure 13

decision
(MPS or LPS)

codestream

internal state
update
(A & C register)
1401

logic

1408

1400

probability class
(Qe_value)

CONTEXT
MODEL
1410

context

memory

1403

probability state

logic
1405

logic

1402

1404

1406

1407

Figure 14A

CODESTREAM

CONTEXT MODEL 1430 → MEMORY 1431 → logic 1432 → Q_e_value → DECODE + A+C UPDATE 1433 → decision

Probability state

Figure 14B.

codestream ──→ [internal state update (A & C register) 1503] ──→ [logic 1504] ──→ pclass1 / 1509 ──→ [> 1511] ──→ [AND 1513] ──→ decision (MPS or LPS)

pclass2 / 1510 ──→ [< 1502]

1501

[context model 1520]: [context 1502] ──→ [memory 1505] ── probability state ──→ [logic 1507] ── probability class (index) 1508

1506

Figure 15

0							
		MPS	MPS	MPS	MPS	MPS	LPS
code	---						
		LPS	LPS	LPS	LPS	LPS	MPS
known state		pclass 0	pclass 1	pclass 2	pclass 3	pclass 4	pclass 5

Figure 16 A

pclass : 0 1 2 3 4 5
result : M M M M L M

[MUX] ──→

Figure 16B

5MPS
4 MPS
3 MPS
2 MPS
1 MPS
LPS

Figure 17

luminance chrominance chrominance

(A)

(B)

(C)

Figure 18

luminance   chrominance   chrominance

(A)

(B)

(C)

Figure 19

luminance   chrominance   chrominance

(A)

(B)

(C)

Figure 20

coded data

length, zero
bitplanes and
coding passes

coded data

length, zero
bitplanes and
coding passes

coded data

length, zero
bitplanes and
coding passes

coded data

length, zero
bitplanes and
coding passes

workspace
memory

coded data memory
(or memories)

Fig. 21

8 bit image data

WAVELET
TRANSFORM

COEFFICIENTS

15,7
14,6
13,5
12,4
11,3
10,2
9,1
8,0

0

8

counters

memory array

Figure 22-A

CONTEXT
MODEL

15,7
14,6
13,5
12,4
11,3
10,2
9,1
8,0

0

8

memory for
VL code

memory for
each coeffcient

Figure 23

addr → MEMORY ARRAY 2201 → 1bit

COUNTER VALUE →

Comparison Logic (addr ≥ counter) 2210

2211

Figure 22B

FIG. 24

FIG. 25A

$-X_0 + 2X_1 - X_2$

2502

2501

1..N+1

1..N+1

0..N 0..N 0..N

0

0

Reversible

Irreversible

FIG. 26A

$X_0 + 4X_1 + X_2$

$X_1 - \left\lfloor \dfrac{X_0 + X_2 + 2}{4} \right\rfloor$

$4X_1 - X_0 + X_2$

Reversible

Irreversible

2604

2603

2602

2601

2602

2602

Rev

Irrev

(rev)

(Irrev)

0..N 0..N 0..N

2..N+2

2..N+2

2..N+2

0..1

FIG. 25B

$$-X_0 + 2X_1 - X_2$$

"ODD"
+ for inverse

L

Reversible

Irreversible

1..N+1

1..N+1

0..N + +

0..N

0..N

0

0

0

FIG. 26B

$$X_0 + 4X_1 + X_2$$

$$X_1 - \left\lfloor \frac{X_0 + X_2 + 2}{4} \right\rfloor$$

"EVEN"
- for inverse

H

Reversible

Irreversible

2..N+3

2..N+2

0..N

0..N

0..N

Rev

Irrev

(rev) 2
(Irrev) 0

2602

0..1

FIG. 27

PIXELS

AB | CD | LINE BUFFER

1LL
AB | CD | Line Buffer
1HL
1LH
1HH

2LL
AB | CD | Line Buffer
2HL
2LH
2HH

3LL
3HL
3LH
3HH

X: ABCD ABCD ABCD...

YES: ABABAB....CDCDCD....

FIG. 28

INVERSE

A	B
C	D

"A"

ODD   2814

1/4 TILE WIDTH
LINE BUFFER   2812

EVEN   2810   "C"

"B"

ODD   2815

1/4 TILE WIDTH
LINE BUFFER   2813

EVEN   2811   "D"

TILE WIDTH 1/2
LINE BUFFER   2808

LINE BUFFER   2809
1/2 TILE WIDTH

HORIZONTAL

LL   2801

HL

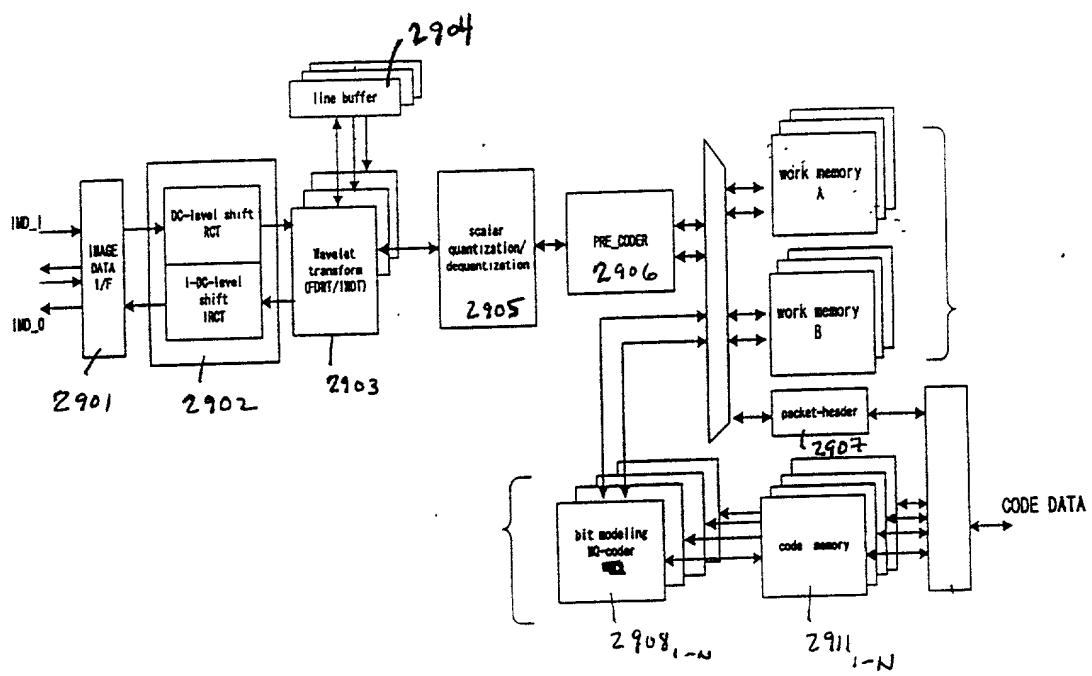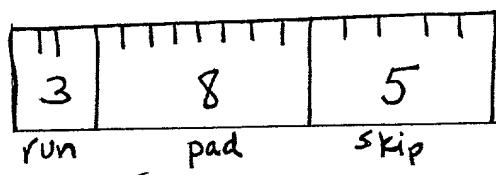EVEN   2815

2807

ODD   2803

LH   2804
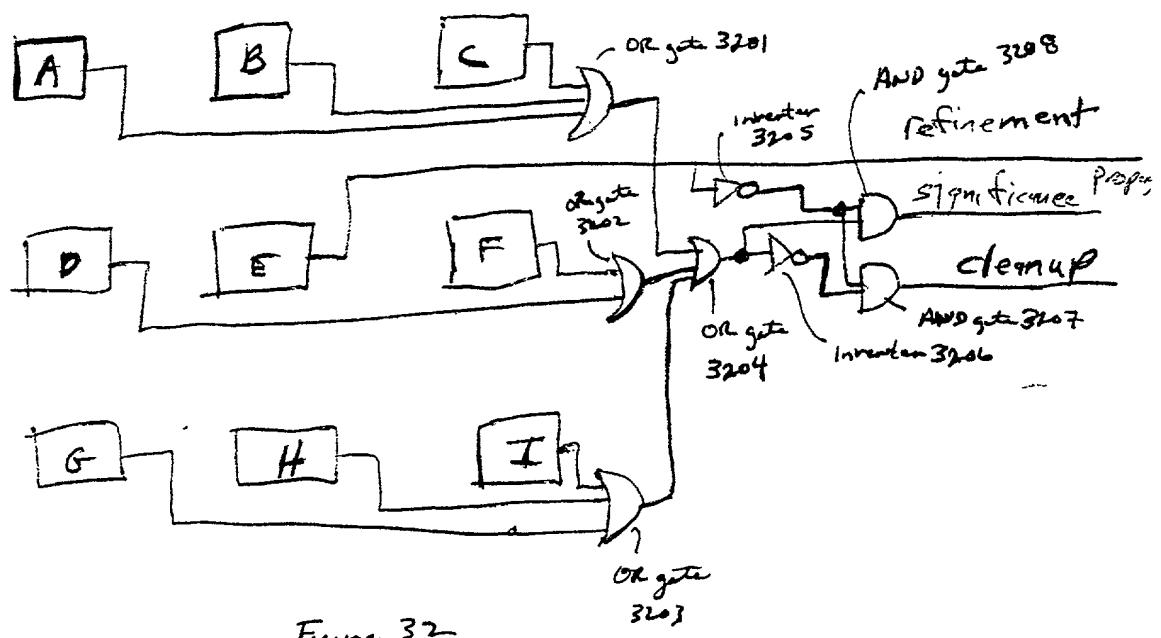
HH

EVEN   2805

2806

ODD

2807

Figure 29

Figure 30

8x 8 region

Figure 31

OR gate 3201
AND gate 3208
refinement
Inverter 3205
significance Proper
OR gate 3202
cleanup
OR gate 3204
AND gate 3207
Inverter 3206

OR gate 3203

Figure 32